**80286 Microprocessor**

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## 80186

We are skipping over the **80186 microprocessor** because it is the same as the 8086 microprocessor, just with four additional components:

1. **Clock Generator** – This is a component we have already seen, an IC that generates clock pulses. The 80186 has this built into the IC.
2. **2 Independent DMA Channels** – We already had one DMA channel, the HOLD and HLDA pins. 80186 allows two such channels (but this could be using the same pair of pins).
3. **Programmable IC** - The 80186 is a programmable IC.
4. **3 Programmable 16-bit Timers**

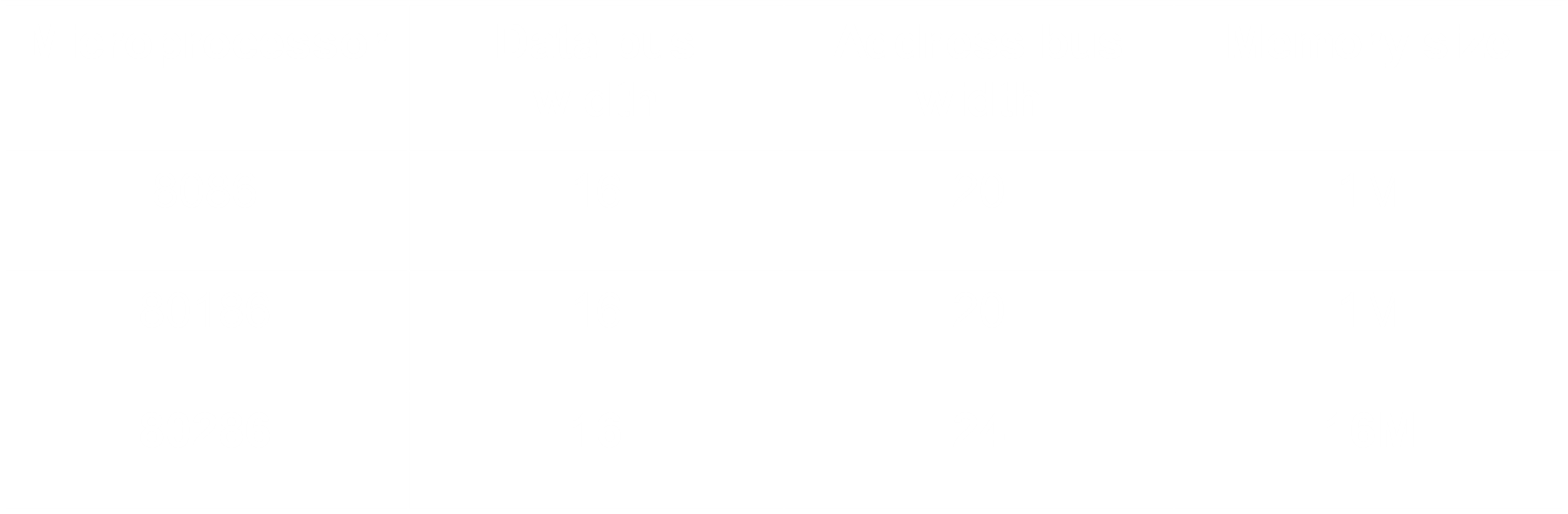
The 80186 is more of a **controller** than a microprocessor. It is used mostly in industrial control applications.

## Salient Features

The Intel 80286 is a high-performance microprocessor with **memory management** and **protection**. It is the first member of the family of advanced microprocessors that has on-chip memory management and protection abilities, primarily designed for multi-user or multitasking systems.

The microprocessor is available in 12.5MHz, 10MHz and 8MHz clock frequencies. It is housed in a **68-pin package** with 134,000 transistors. These pins are **non-multiplexed**, meaning there are 24 pins for the address bus and a separate 16 pins for the data bus.

With regards to memory, the 80286 has a **24-bit address bus**, which allows addressing of **16MB of physical memory**. The **data bus** is still of 16 bits. If we compare this with previous microprocessors:



### Virtual Memory

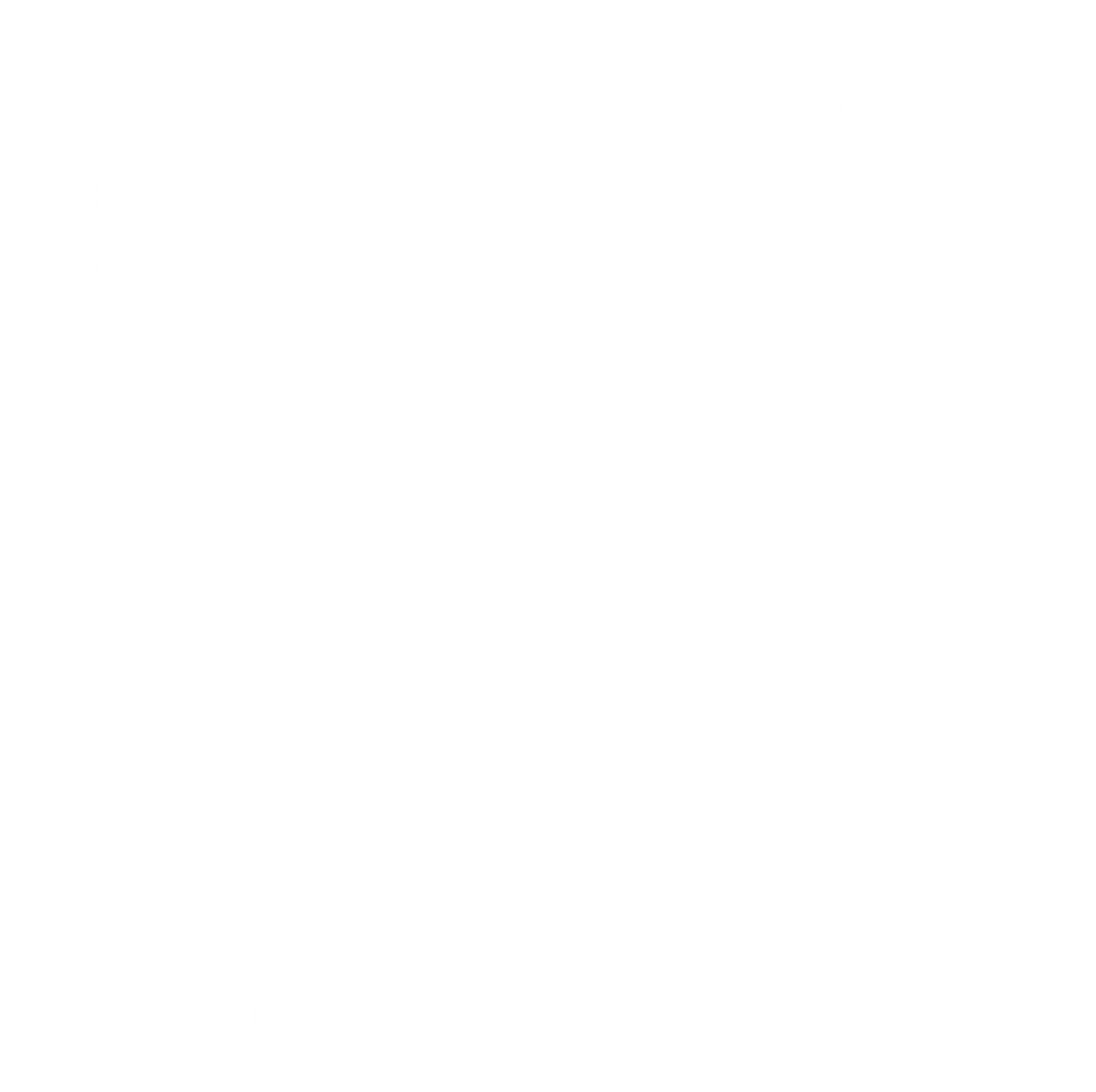
80286 also introduces the concept of **virtual memory**. This is when a program requires **more RAM than is available**, so space from the secondary storage, the hard disk, is allocated for its use. There is **1GB** of virtual memory for each task.

### Operating Modes

The Intel 80286 has **two operating modes**.

The first is called the **Real Address Mode**. In this mode, the 80286 is just a **fast 8086**, up to 6 times faster, with memory management and protection mechanisms disabled. This allows the microprocessor to only address the first **1MB of memory space**. This 1MB is called the **real memory**, **conventional memory** or **DOS memory system**. The concepts of **segments** and **offsets** come into play here.

Note that, for Real Address Mode, the operations are exactly like 8086, but the memory has **6 bytes per location**.



Windows does not use the real address mode since it requires more than 1MB of memory. This brings us to the second operating mode, the **Protected Virtual Address Mode**. In this mode, the 80286 operates with all its **memory management and protection capabilities** with the advanced instruction set. Since all **24 address lines** are used, the complete **16 MB** of physical memory and **1 GB** of virtual memory can be used.

### Multitasking

The 80286 includes some **special instructions**, such as to allow the operating system to perform **multitasking**. If a new task with a higher priority needs to be performed, the microprocessor does the following:

1. End the current task
2. Save its states
3. Switch to the new task
4. Load its states
5. Begin executing the new task

This is very similar to how **interrupts** work. The difference is that interrupts are treated as high priority tasks, and in multitasking, we simply use **privilege levels** for tasks.

There are **four privilege levels**, 00, 01, 10 and 11, going from highest priority to lowest.

## Memory Management Unit

The **memory management unit** allows the 80286 to switch to **protected mode** and start using **virtual memory**.

Here, we are no longer using segments, but instead, a **16-bit selector**. The selector is used to select a **descriptor** for the **desired segment** in a table of descriptors.

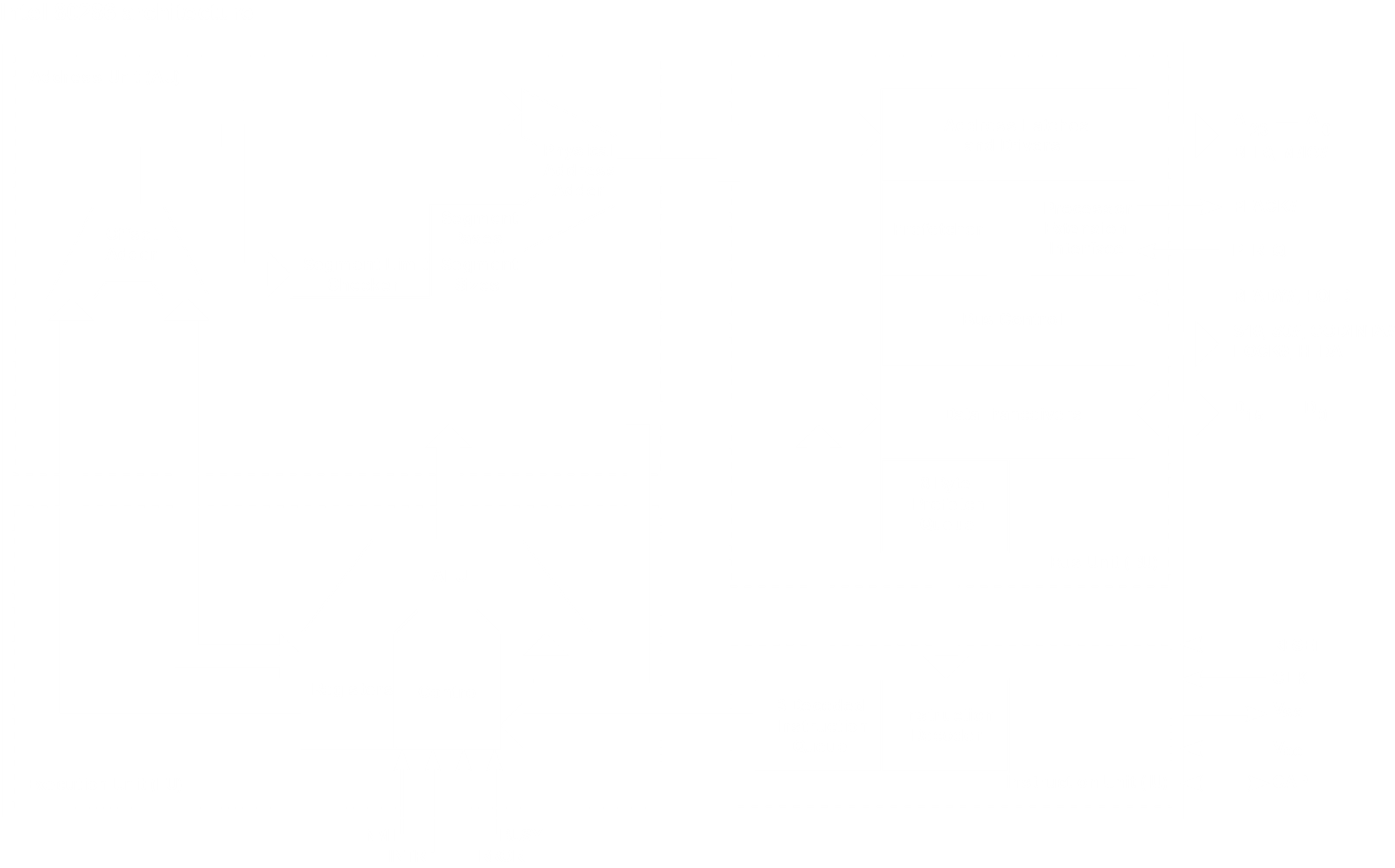
Each descriptor describes a **64 KB** memory segment, and there are **16,000 descriptors** in total, which brings the maximum addressable virtual memory up to **1GB**.

The descriptor contains a **24-bit physical address**. For the selected segment, a **16-bit offset** is also used to access a specific location.

We will look into specific examples of how to use this mechanism later on.

## Internal Block Diagram

The 80286 has four sections, the **Execution Unit** and the **Bus Unit** that were present in the 8086 are still present here, but the **Address Unit** and the **Instruction Unit** have been added.



The **Address Unit** deals with deriving physical addresses. This requires a separate unit because of the two **operation modes**. Again, the exact process of how the address is generated will be discussed later on.

Next comes the **Bus Unit**, which is responsible for all external communication. The address generated by the Address Unit enters the **Address Latches and Drivers** section of the Bus Unit. From here, it goes out through the **Address Bus**. The data is received through the **Data Bus** and enters the **Data Transceivers** section.

Notice that the **Bus Unit** has a **6-Byte Prefetch Queue** section. This means that while the microprocessor is executing something, 6 more bytes worth of data have been prefetched for the next instructions. This is why this microprocessor is 6 times faster than the 8086.

From the 6-Byte Prefetch Queue, instructions enter the **Instruction Decoder**, which is in the **Instruction Unit**. There is an **Instruction Queue** here, similar to the one from the 8086. Decoded instructions go to the **Execution Unit**.

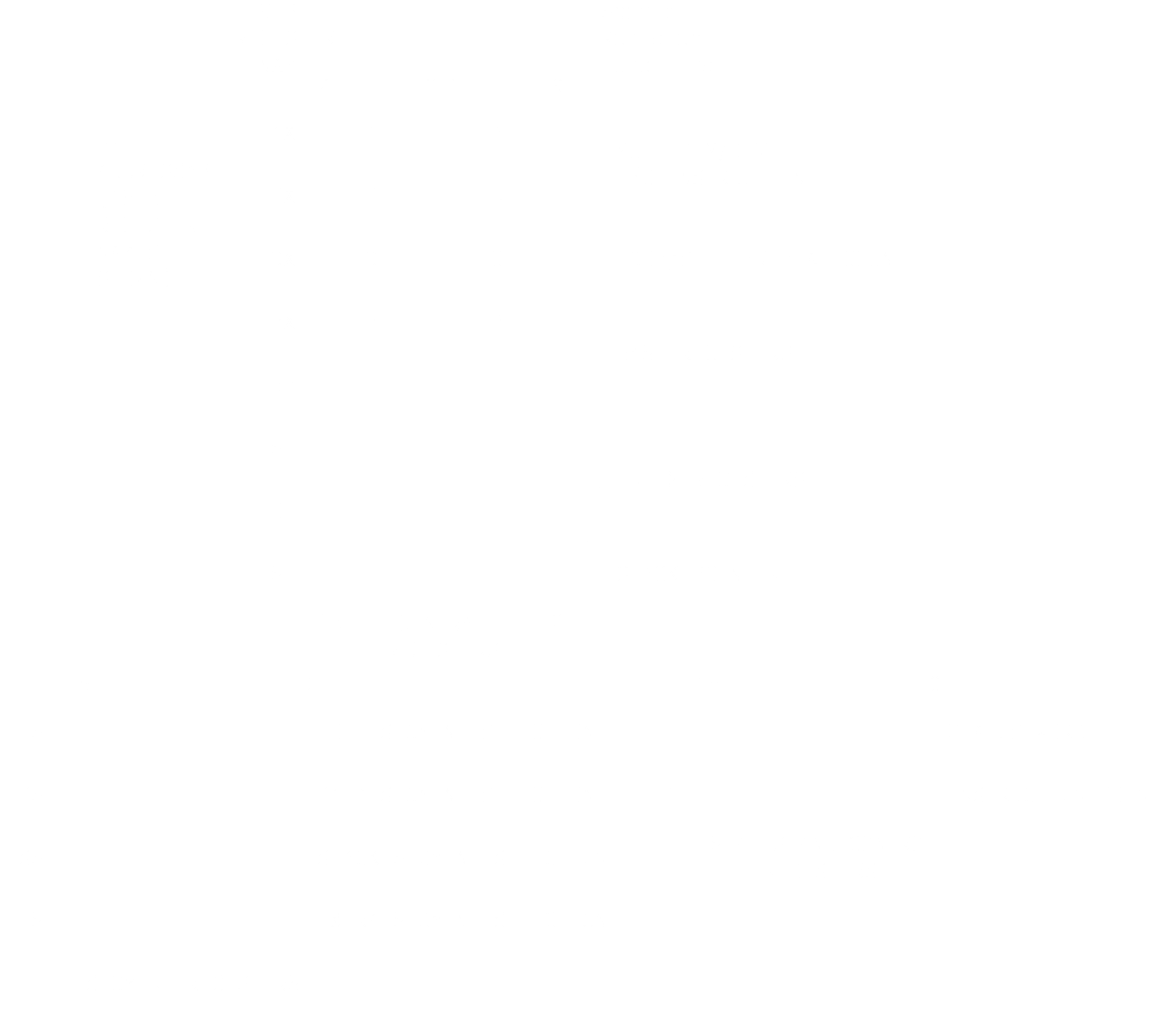
In the **Execution Unit**, the main parts are the **Register Bank**, the **ALU** and the **Control Unit**. There is an additional special **16-bit register** called the **Machine Status Word** (MSW). The Register Bank and MSW are discussed in depth below.

The Reset, Clock and Power Supplies are connected to the **Instruction Unit**. **Interrupts** and **Errors** are connected directly to the **Execution Unit**.

## Register Organization

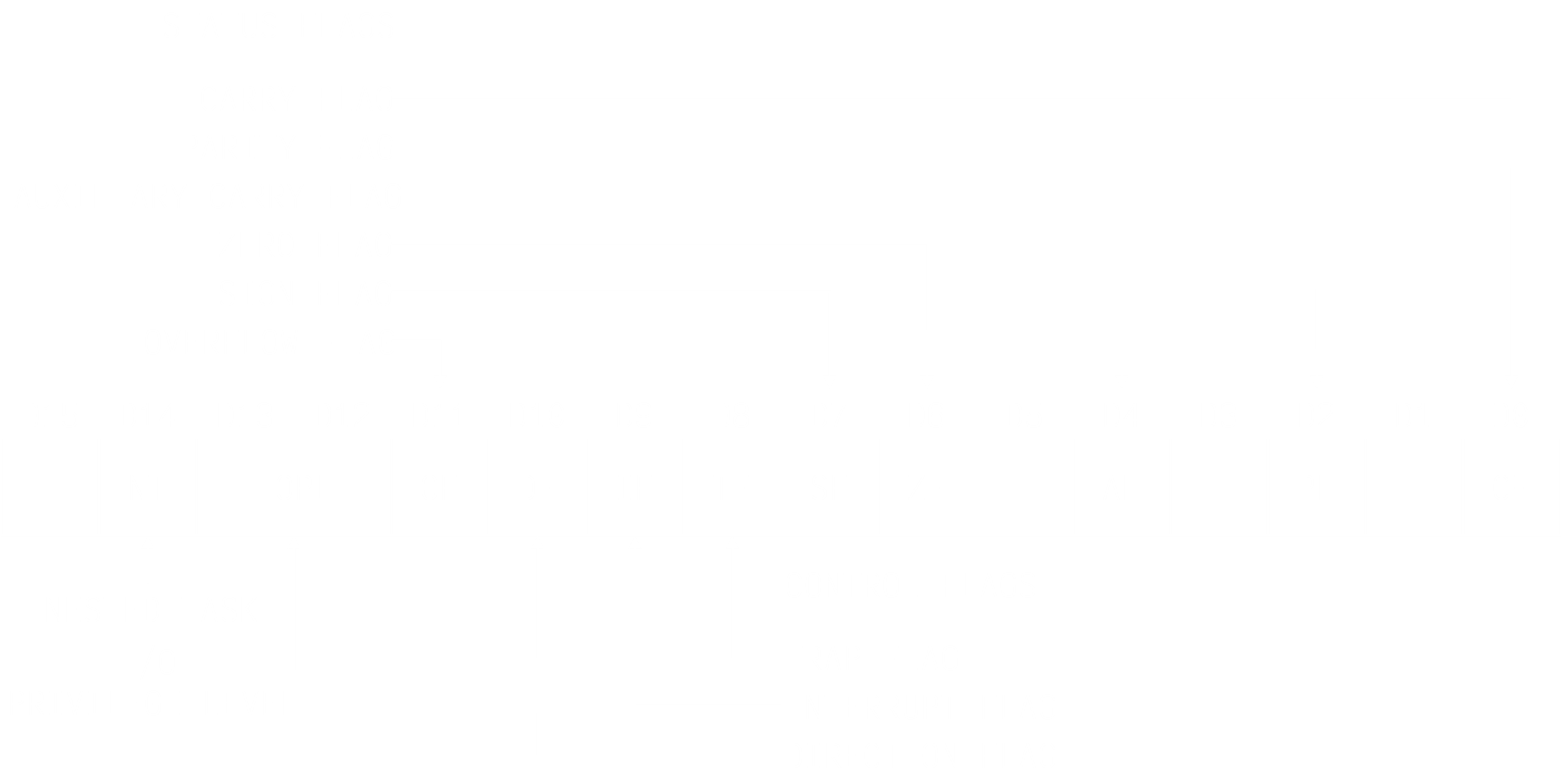
The 80286 has the same registers that the 8086 has:

* 8 16-bit General Purpose Registers – Data registers, Base registers, Pointer registers and Index registers
* 4 16-bit Segment Registers
* Status and Control Registers
* Instruction Pointer



### Flags

The **Flag Register** has some changes in it though.



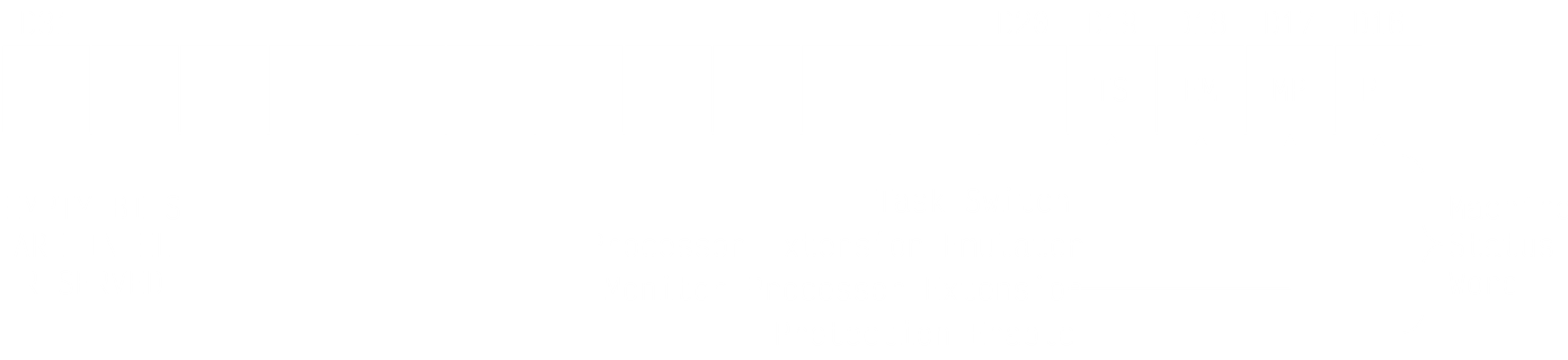
The **Nested Task** (NT) and **I/O Privilege Level** (IOPL) flags are new.

The IOPL flag uses **two bits** and defines one of the privilege levels previously mentioned for the current task.

If a task with a higher privilege level arrives while one with a lower privilege level is executing, the old task is suspended and the new task is executed. In this scenario, the new task is called a **nested task**. The NT flag indicates that the current task is a nested task.

### Machine Status Word

The only new register is the **Machine Status Word** (MSW).



Even though it has 16 bits, only the **lower 4 bits** are used as four **flags**:

* **Protection Enable** (PE) – This indicates that the microprocessor is running in Protected Virtual Mode.
* **Monitor Processor Extension** (MP) – Microprocessors can have **co-processors**, which are connected to the main processor, to assist in some activities. If the co-processor is being monitored, this flag is set.
* **Processor Extension Emulator** (EM) – Instead of using a co-processor, the microprocessor can divide itself and work in separate parts as though one part were a co-processor. In this scenario, this flag is set.
* **Task Switch** (TS) – This flag is set if the microprocessor is currently switching from one task to another.